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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,668	01/17/2002	Patrick L. Connor	PW 0249740 P12832	1163

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EXAMINER	
PATEL, NIRAV B	

ART UNIT	PAPER NUMBER
2135	

DATE MAILED: 08/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/051,668	CONNOR ET AL.	
	Examiner	Art Unit	
	Nirav Patel	2135	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2006 (Amendment)*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *8-13,16,18,19,21,22,24,25,27,32 and 33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-13, 16, 18, 19, 21, 22, 24, 25, 27, 32 and 33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment filed on May 26, 2006 has been entered.

2. Claims 8-13, 16, 18, 19, 21, 22, 24, 25, 27, 32 and 33 are pending. Claims 1-7, 14, 15, 17, 20, 23, 26, 28-30 and 31 are cancelled by the applicant and claims 8, 16, 22 and 27 are also amended by the applicant. Claims 32 and 33 are newly added claims by the applicant.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 8-13, 16, 18, 19, 21, 22, 24, 25, 27, 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishna, Suresh (WO 01/05086) and in view of Johnson et al (US Patent No. 6,754,755).

As per claim 8, Krishna discloses:

host memory to store the encrypted packet after receipt by the computing system **[Fig. 1A, 1B, page 7 lines 34-35]**, a controller to perform said decryption operation **[Fig. 1A, 1B, component 102 or 152, Fig. 3, 6A, page 9 lines 1-2, page 18 lines 30-31]**, a bus providing electronic communication among said host memory and said controller **[Fig.**

1A, 1B, page 7 lines 16-20]. Krishna teaches that receiving the packets from the LAN or WAN, and **storing the packets to the memory 166 and transferring to the chip 152** on the service module 153 for **security processing (e.g. decryption/authentication)**. The processed packets are then **sent back over the matrix 154 through the memory 166 [Fig. 1B, 6A, page 7 lines 34-36, page 8 lines 1-2, page 18 lines 30-31]**. Krishna mentions raising the interrupt **[page 26 and 20]**. Krishna doesn't expressively mention the assertion of the interrupt.

Johnson teaches:

a network driver to regulate the various operation and to transmit a command **[Fig. 5, 6 col. 11 lines 63-66]**, the controller asserting an interrupt *prior to a complete transfer* of said decrypted packet (i.e. packet) from said controller to said host memory **[Fig. 2, col. 8 lines 51-55]**, wherein the controller waits the average latency value (i.e. delay time) before said assertion of the interrupt in response to said command **[col. 9 lines 22-40, *i.e. determining the interrupt latency period to calculate delay time and asserting the early interrupt, after the expiration of the delay time*, col. 11 lines 63-67, col. 12 line 1, i.e. *asserting the interrupt in response to the command*]**.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Johnson with Krishna, since one would have been motivated to improve network processing between the network adapter or NIC and its host computer **[Johnson, col. 4 lines 26-28]**.

As per claim 9, the rejection of claim 8 is incorporated and further Krishna teaches: network interface to provide electronic communication between said computer and a network **[*page 6 lines 16-18* "as shown in Fig. 1, the cryptography acceleration chip 102 may be part of an otherwise standard network line card 103 which includes a WAN interface 112 that connects the processing system 100 to a WAN, such as the internet"]**.

As per claim 10, the rejection of claim 9 is incorporated and further Krishna discloses: security association (SA) is stored in said host memory **[*page 11 lines 8-10* "the chip also includes various buffers 210 for storing packet data, security association information" Fig. 3]**.

As per claim 11, the rejection of claim 10 is incorporated and further Krishna discloses: network driver parses said encrypted packet, matches said encrypted packet with one of said at least one SA **[*page 11 lines 18-20* "packet header information is sent to a packet classifier unit 204 where a classification engine rapidly determines security association information required for processing the packet"]** and instructs said network interface to transfer said encrypted packet and said one SA across said bus to said controller **[*page 11 lines 31-33* "the packet distributor unit 306 then distributes the security association information(SA) received from the packet**

classifier unit 304 and the packet data via the internal bus 305 among a plurality of cryptography processing engines 316" Fig. 6A].

As per claim 12, the rejection of claim 8 is incorporated and further Krishna discloses: network interface includes a cryptography accelerator **[*page 6 lines 16-17* "as shown in Fig. 1, the cryptography acceleration chip 102 may be part of an otherwise standard network line card 103 which includes a WAN interface 112"]**.

As per claim 13, the rejection of claim 8 is incorporated and further Krishna discloses: controller transfers said decrypted packet across said bus from said controller to said host memory **[*page 7 line 36, page 8 line 1* "the processed packet are then sent back over the matrix 154, through the memory 166"]**.

As per claim 16, it encompasses limitations that are similar to limitations of claim 8. Thus, it is rejected with the same rationale applied against claim 8 above.

As per claim 18, the rejection of claim 16 is incorporated and further claim 18 is a method claim corresponds to system claim 11 and is rejected for the same reason set forth in the rejection of claim 11 above.

As per claim 19, the rejection of claim 16 is incorporated and further Krishna teaches:

step of converting said encrypted packet to said decrypted packet further includes authenticating said decrypted packet **[Fig. 6A *page 9 lines 9-10* "then pass the packet along to one of the four cryptography and authentication engines 214"].**

As per claim 21, the rejection of claim 16 is incorporated and further Krishna teaches: indicating decrypted packet to a protocol stack **[Fig. 3 component 318 output FIFO (MAC) *page 12 lines 16-17* "the packet distributor 306 control the output FIFO 318 to ensure that packet ordering (i.e. Per-flow ordering) is maintained", *page 9 lines 31-35* "Per-flow ordering offers a good trade-off between maximizing end-to-end system performance (specifically desktop PC TCP/IP stack)"]**. Johnson teaches asserting the early interrupt (i.e. after expiration of the delay time) [col. 9 lines 37-38]. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Johnson with Krishna, since one would have been motivated to improve network processing between the network adapter or NIC and its host computer **[Johnson, col. 4 lines 26-28]**. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Johnson with Krishna, and the combination teaches indicating decrypted packet to a protocol stack after asserting said interrupt.

As per claim 22, it is a device claim corresponds to method claim 16 and is rejected for the same reason set forth in the rejection of claim 16 above. Further Krishna teaches:

a machine-readable storage medium; and machine-readable program code, stored on the machine-readable storage medium **[*page 12 lines 5-6* "a processor which controls the sequencing and processing of the packets according to microcode stored on the chip"]**.

As per claim 24, the rejection of claim 22 is incorporated and it encompasses limitations that are similar to limitations of claim 11. Thus, it is rejected with the same rationale applied against claim 11 above.

As per claim 25, the rejection of claim 22 is incorporated and it encompasses limitations that are similar to limitations of claim 19. Thus, it is rejected with the same rationale applied against claim 19 above.

As per claim 27, the rejection of claim 22 is incorporated and it encompasses limitations that are similar to limitations of claim 21. Thus, it is rejected with the same rationale applied against claim 21 above.

As per claim 32, the rejection of claim 16 is incorporated and Krishna teaches the encrypted packet is fully decrypted **[Fig. 6A, page 18 lines 30-31]**. Johnson teaches asserting the early interrupt (i.e. after expiration of the delay time) **[col. 9 lines 37-38].** Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Johnson with Krishna, since one would have been

motivated to improve network processing between the network adapter or NIC and its host computer **[Johnson, col. 4 lines 26-28].** Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Johnson with Krishna, and the combination teaches asserting the interrupt before the encrypted packet is fully decrypted.

As per claim 33, the rejection of claim 22 is incorporated and it encompasses limitations that are similar to limitations of claim 32. Thus, it is rejected with the same rationale applied against claim 32 above.

Response to Amendment

4. Applicant has amended claims 8, 16, 22 and 27 which necessitated new ground of rejection. See rejection above.

5. Applicant's arguments filed May 26, 2006 have been fully considered but they are not persuasive.

Examiner has considered the applicant's amendment and remarks, and maintains that the cited prior art (combination of Krishna and Johnson) still teaches the amended claimed limitation. Refer further remarks as below.

Applicant argues that:

The examiner has not identified that a command has been issued to a controller. Johnson doesn't disclose a method including **waiting for the average latency value**

before said assertion of an interrupt in response to said decryption command and the interrupt is **asserted at a time before** completing said transfer. Further, the applicant argues, the average latency as claimed in the present invention is not the same as the approximate interrupt latency as taught by Johnson.

Examiner disagrees with applicant's remark and still maintains that:

Krishna's invention related to provide the security process to the data packets using the cryptography accelerator chip. The cryptography accelerator chip is incorporated on network line card. The cryptographic accelerator chip on the card has associated with it a local processing unit and local memory **[Fig. 1A, 1B]**. Krishna teaches that receiving the packets from the LAN or WAN, and **storing the packets to the memory 166 and transferring to the chip 152** on the service module 153 for **security processing (e.g. decryption/authentication)**. The processed packets are then **sent back over the matrix 154 through the memory 166 [Fig. 1B, 6A, page 7 lines 34-36, page 8 lines 1-2, page 18 lines 30-31].** The crypto engine performs encryption/decryption, authentication/digital signature processing and compression/decompression processing **[Fig. 2, page 11 lines 34-35, page 12 lines 1-2].**

Johnson's invention relates to requesting services of a processor of a computer. Johnson discloses a network controller system with interrupt inhibits, which improves network processing between a network adapter or NIC and its host computer. The network logic as shown in Fig. 5, which is transmitting and receiving the data (i.e. packet) and handling data transfer to and from the memory **[Fig. 5, col. 11 lines 63-65]**.

The network logic is further, **receiving and executing commands from the driver [Fig. 5, col. 11 lines 65-66].** Therefore, the combination of Krishna and Johnson teaches transmitting the command to the controller and performing the decryption process as above.

Further, Johnson discloses determining an approximate interrupt latency period of the computer system on the network and cause the interrupt logic of the NIC to assert the interrupt early by the approximate latency period (i.e. early interrupt) **[col. 9 lines 22-26]**. The NIC asserts the interrupt early, after the expiration of the delay time **[col. 9 lines 37-38** ***i.e. determining the interrupt latency period to calculate delay time and asserting the early interrupt (asserting at a time before), after the expiration of the delay time*****, col. 11 lines 63-67, col. 12 line 1, i.e.** ***asserting the interrupt in response to the command*****].** Furthermore, the examiner recognizes that obviousness can only be established by combining or modifying the teaching of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to on of ordinary skill in the art. See *In re Fine*, 837 F. 2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re* Jones, 958 F.2d 347, 21 USPQ 2nd 1941 (Fed. Cir 1992). In this case, the combination of Krishna and Johnson teaches the claimed subject matter and the combination is sufficient.

From the examiner point of view the cited reference clearly teaches the average latency value as above. The argued term "average latency value" must be clearly defined in the claimed language, if Applicant believes it differs from the cited one. Applicant is

reminded that additional modification to clarify the claimed language is necessary for further consideration and distinction from the prior art.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Brcich et al. (US Patent No. 6,304,911) --- Information Packet reception indicator for reducing the utilization of a host system processor unit.

Johnson (US Patent No. 5,905,874) --- Method and System for reducing data transfer latency when transferring data form a network to a computer system.

Rodrigues et al (US 6,715,005) – Method and system for reducing latency in message passing systems.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nirav Patel whose telephone number is 571-272-5936. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Vu can be reached on 571-272-3859. The fax and phone numbers for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2100.

NBP
8/18/06

KIM VU
SUPERVISORY PATENT EXAMINER
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